

In re Appln. of ABE et al.
Application No. 10/892,539

AMENDMENTS TO THE DRAWINGS

The attached sheets include changes to Fig. 9-21 and 29-35.

The changes proposed to the drawings in the Preliminary Amendment are made in the attached drawing sheets. In addition, the section line in Figure 9 indicating the location of the section to produce Figure 10 is corrected.

Attachment: Replacement Sheet(s)

REMARKS

In response to the Official Action mailed August 19, 2003, Applicants amend their application and request reconsideration. In this Amendment the method claims 13-15, which are not being examined, are cancelled. No other claims are added or cancelled so that claims 1-12 remain pending. Of these claims, claims 1-3 and 5-7 have been examined pursuant to a species election requirement and an election. Although claim 4 has been withdrawn from examination, it depends from claim 1, which is generic to claims 1-7.

A PTO-1449 form indicating consideration of the publications filed December 10, 2002 was returned with the Official Action. A single reference, JP-2000-156464, was cited in an Information Disclosure Statement filed simultaneously with the patent application. The PTO-1449 form filed with that Information Disclosure Statement has not been returned and an additional copy is attached for the Examiner's convenience.

In response to the comments concerning the drawings, formal drawing sheets incorporating the amendments proposed in the Preliminary Amendment are supplied. In addition, in view of the Examiner's explanation, the section line in Figure 9 indicating the section taken to produce Figure 10 is relocated to be consistent with Figure 10. That section line passes between the lower semiconductor chip 1b and the die pad 4b. The original section line of Figure 9 was inadvertently located to indicate that the section passed through the die pad 4b, which is inconsistent with the Figure 10 that was supplied with the patent application. The amendment resolves the issue surrounding this minor error in location of the section line.

The invention as described by the claims under examination concerns an arrangement of two semiconductor chips within a single resin encapsulated package. Terminal electrodes surround side surfaces of one of the semiconductor chips and the semiconductor chips are stacked on each other. A plan view of this structure is taken perpendicular to the largest area of the semiconductor chips, i.e., along the direction of the stacking of the semiconductor chips. Claim 1 has been amended to clarify the direction of the plan view, although the direction is plainly clear from the application as filed.

An important feature of the invention as defined by claim 1 is that the terminal electrodes that are connected by wires to the two semiconductor chips are located entirely outside the region where the semiconductor chips are located. Again, for clarity, the description of this feature of the invention is moved from the first paragraph of claim 1 to the final paragraph of that claim.

The dependent claims are amended, as necessary, to conform to the amendment of claim 1. The transverse arrangement of the two semiconductor chips that are stacked and that is

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described in claim 6 is described with greater clarity in the amended form of that claim. Essentially, no claim has been amended substantively; the claims have merely been amended for clarity.

Claims 1-3 were rejected pursuant to 35 USC 102(e) as anticipated by Choi et al. (U.S. Patent 6,075,284, hereinafter Choi). Since Choi issued approximately two weeks before the filing of the present patent application, it is believed the Examiner intended to cite a difference subsection of 35 USC 102 as the legal basis of the rejection. In any event, the rejection is respectfully traversed.

In making the rejection, the Examiner characterized Figure 13 of Choi as a plan view. It is apparent that that figure is a side view. To avoid dwelling upon the definition of various views, the claims have been clarified so that Figure 13 of Choi can no longer be considered the view referred to in the claims. Further, it is apparent that in Choi that the terminal electrodes are not entirely outside the area in which the semiconductor chips are located. Because of at least these two differences, Choi cannot anticipate any of claims 1-3 or any of claims 4-7.

Claims 1-3 and 5-7 were rejected pursuant to 35 USC 102(e) as anticipated by Song et al. (U.S. Patent 5,770,888, hereinafter Song). Because Song issued slightly more than two years before the filing of the present patent application, it is believed that a different subsection of 35 USC 102 was relied upon as the legal basis of the rejection. The rejection is respectfully traversed.

It is sufficient to point out that the terminal electrodes of Song, namely elements 22, are not entirely outside the area occupied by the upper and lower semiconductor chips when viewed along a direction of stacking of those semiconductor chips. The regions 22a of the terminal electrodes are clearly between pairs of the semiconductor chips. Therefore, Song cannot anticipate any pending claim.

With regard to claim 2, it is apparent that there are no die pads employed in the structures of either Choi or Song. Choi employs extending parts of the terminal electrodes to support the semiconductor chip. Those extending parts are not a die pad. Song has no element corresponding to a die pad.

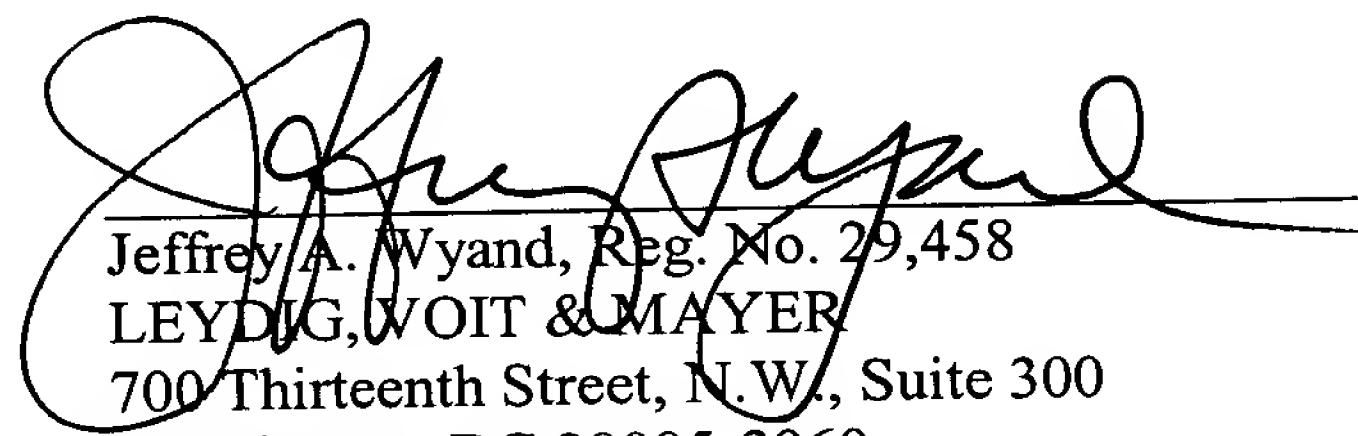
With regard to claim 6, neither Choi nor Song illustrates the arrangement with the two semiconductor chips being rectangular and “crossed” with each other as in the invention. Thus, at least claims 2 and 6 additionally distinguished from the two references applied in rejecting claim 1.

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Since claim 1 is clearly in form for allowance, claim 4 should be rejoined to the prosecution pursuant to 37 CFR 1.141.

Reconsideration and allowance of at least claims 1-7 are earnestly solicited.

Respectfully submitted,



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